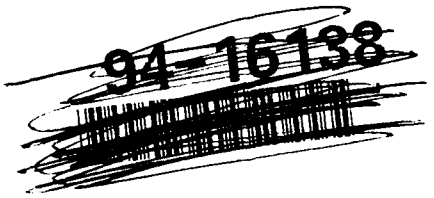
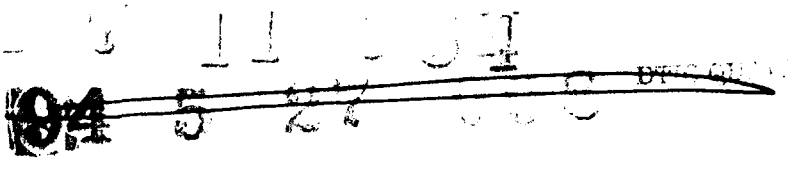
Japanese Advanced Semiconductor Manufacturing

June 1, 1992



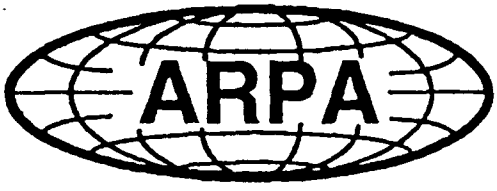
Trip Report of ARPA Technology Assessment Team

Zachary J. Lemnios (ARPA/MTO) (703) 696-2278
Nicholas J. Naclerio (ARPA/ESTO) (703) 696-2216
Yoon Soo Park (ONR) (703) 696-4715



31816

Japanese Advanced Semiconductor Manufacturing



June 1, 1992

Trip Report of ARPA Technology Assessment Team

Zachary J. Lemnios (ARPA/MTO) (703) 696-2278
Nicholas J. Naclerio (ARPA/ESTO) (703) 696-2216
Yoon Soo Park (ONR) (703) 696-4715

[redacted]

Table of Contents

List of Acronyms

AGV	automated guided vehicle
ARPA	Advanced Research Projects Agency
ASIC	application-specific integrated circuit
CAD	computer-aided design
CCD	charge-coupled device
CIM	computer-integrated manufacturing
CMOS	complementary metal-oxide-semiconductor
CVD	chemical vapor deposition
DRAM	dynamic random access memory
DUV	deep ultra-violet wavelengths
EIAJ	Electronics Industries Association of Japan
GaAs	gallium-arsenide
HEMT	high electron mobility transistor
IC	integrated circuit
kb	a capacity of approximately 10^3 (actually 1,024) bits
LSI	large-scale integration
Mb	a capacity of approximately 10^6 (actually 1,048,576) bits
MMST	Microelectronics Manufacturing Science and Technology
MOCVD	metal-organic chemical vapor deposition
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MPU	microprocessor unit
ONR	Office of Naval Research
PBX	private branch exchange
R&D	research and development
RIE	reactive ion etch
SAW	surface acoustic wave
SEMATECH	Semiconductor Manufacturing Technology Consortium
SEMI	Semiconductor Equipment and Materials International
SMIF	semiconductor mechanical interface [standard]
SOI	silicon-on-insulator
SRAM	static random access memory
TPM	Total Product Maintenance
VRAM	video random access memory

Executive Summary

During the week of April 5 through 9, 1993 an ARPA technology assessment team visited four Japanese semiconductor companies and one Japanese university to evaluate Japanese trends in flexible manufacturing and assess their strategic direction. Of the manufacturing facilities visited, the Mitsubishi 16Mb DRAM facility in Saijo was the most advanced and provided good insight into the Japanese manufacturing directions.

The following key observations and trends of this trip are summarized here and discussed further in this report.

1) All of the manufacturing sites (excluding Tohoku University) are on the classic mega-fab trend which will result in the multi-billion dollar next-generation facilities. Although several of the companies visited knew of the MMST program, we saw no evidence of an analogous Japanese program.

2) Contrary to US manufacturers, the Japanese manufacturers have little concern over the capability and cost of lithography tools and processes. Each of the Japanese companies relied upon local Japanese suppliers (Canon, Nikon) to provide capable tools. Typical 0.5 micron production is accomplished with i-line optical steppers. The lithography tools seen in the factories are one generation older than those typically used by the US.

3) There appears to be very little pre-competitive cooperation among the semiconductor companies, even in development of new tools. There is some support for standards though, mainly through the Electronics Industries Association of Japan (EIAJ) and the worldwide organization of Semiconductor Equipment and Materials International (SEMI).

4) The most advanced manufacturing concepts were seen at Tohoku University under Professor Ohmi. However, few of the ideas proposed by Tohoku University have been implemented into industry.

5) Although the US has far superior computer technology than what was viewed in the Japanese factories, the Japanese have much more pervasive implementation on the manufacturing floor. Even the tools on Toshiba's oldest line were computerized for automatic recipe download.

6) The Japanese companies which were visited each have extensive foreign technology partnerships which include back end of line processing, packaging and final test. This has enabled the Japanese manufacturers to penetrate markets which restrict traditional "foreign suppliers".

6) Japan has fewer restrictions and regulations concerning environmental and safety issues, enabling construction of facilities with less expensive and restricting technology.

1.0 Mitsubishi Electric Corporation Saijo, Shikoku Island

The Mitsubishi facility in Saijo, located on Shikoku Island was visited on April 5, 1993. The Saijo site is Mitsubishi's prime manufacturing site. Complete production, from wafer fabrication to packaging and shipping are done here. Mitsubishi has three other semiconductor factories in Japan, located in Kochi, Fukuoka, and Kumamoto. World-wide, Mitsubishi has built 6 wafer fab lines that are nearly completely automated and computerized. The seventh automated facility is under construction at Saijo. Main products in Saijo are 1Mb DRAM, MPU, 256kb SRAM, VRAM, 4Mb DRAM, and 16Mb DRAM. The ARPA team was able to visit the newest fully operational line, now manufacturing 4 and 16Mb DRAM product, and also was able to see the area designated for a new 16Mb line. The total capacity of the operational, fully automated 16Mb line viewed was about 25,000 wafer starts per month.

1.1 Manufacturing Site Description

The Saijo site consists of three fabrication lines in three separate buildings. Building B is the oldest, having opened in 1985 making 256kb DRAM but is now making 1Mb DRAM at 1 μm geometries with 5 inch wafer diameters. Building B is 140 m by 70 m in three floors.

Building C is identical to building B in size and opened in May, 1985. It is equipped to manufacture products with 1 μm geometry. Presently, it is producing MPU, SRAM, and VRAM products.

The newest facility, building A, opened in 1991. Building A contains 5 floors and measures 220 meters by 50 meters and is used to manufacture 16 and 4 Mb DRAM products with 0.8-0.5 μm geometries in a class 1 environment. While building A can support four fabrication areas, it presently contains just the one 6 inch line. Mitsubishi plans to transfer all 4Mb DRAM processing to Kochi and begin 4Mb SRAM processing in building A. Mitsubishi also plans to upgrade the steppers and etchers in the C lines for 0.7 μm geometries.

The site plan showed a future D building, but Mitsubishi claimed to have no real plans for expansion yet. Their first priority is to complete building A, where a new line "floor 2" is under construction. Floor 2 appears to be identical in floor space area to floor one. This line will be equipped to process 16 Mb DRAM products on 8 inch wafer diameters.

1.2 Facility Description

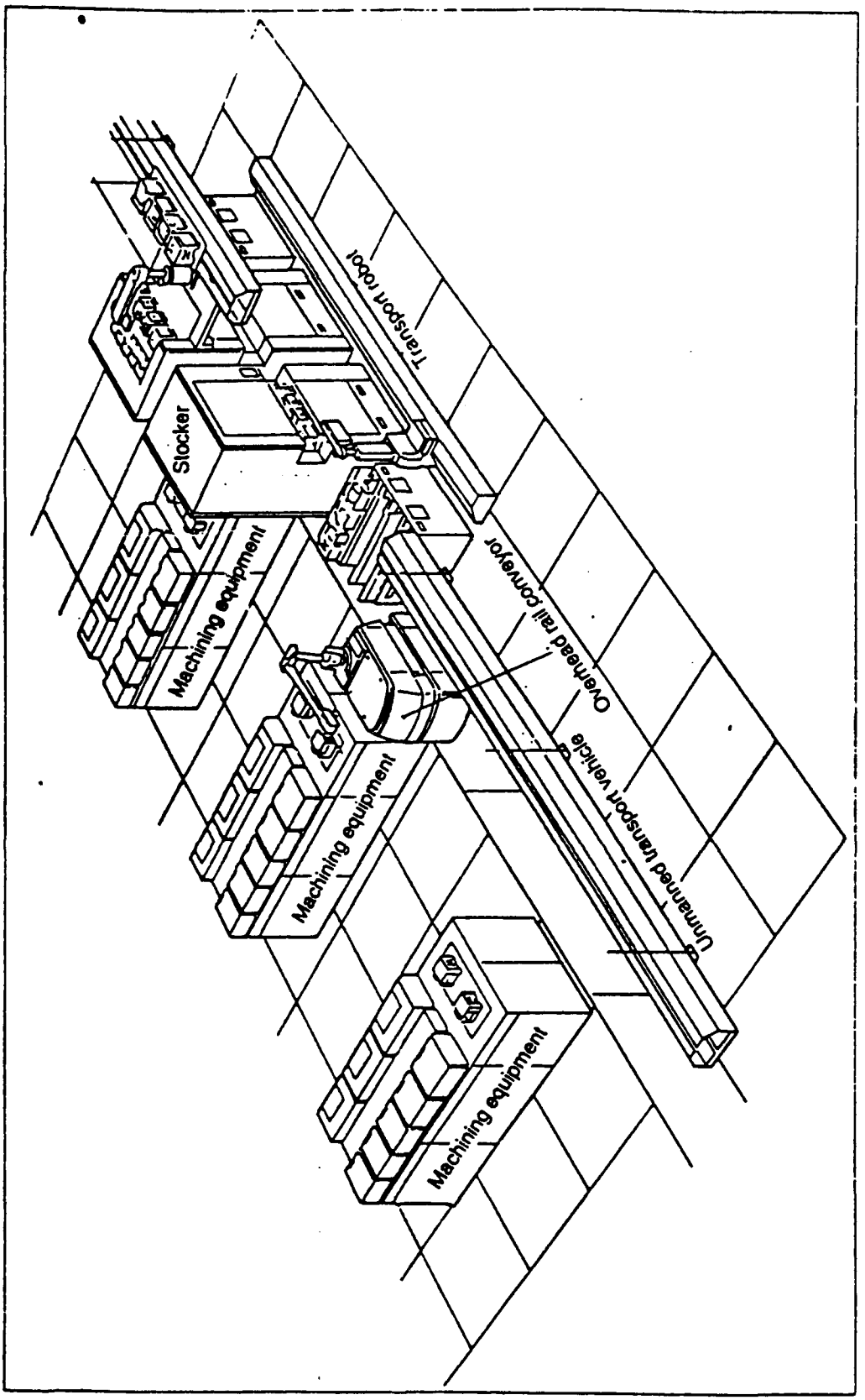
The factory is organized into 5 departments under the General Manager (M. Amano). The 5 departments are General Affairs, Manufacturing Planning, Wafer Manufacturing A (B&C lines), Wafer Manufacturing B (A lines), and

Assembly Manufacturing. About 1,600 people are employed at the plant, approximately 10% are engineers or scientists. About half of the total work force were Mitsubishi employees, the rest were on-site sub-contractors supporting both fabrication and back-end operations. The entire facility runs 24 hours per day on 3 shifts. Building A operates on 3 shifts of approximately 50 people each. The main function of the people is for maintenance and assists, resetting the material transfer robots. Mitsubishi reported to SEMATECH that the automation had reduced the number of people in the clean room by 50%. The total cost of the 6" wafer line was estimated by Mitsubishi to be $600 million. The total cost of the 8" line under construction will be about $1.4 billion.

The team was given an extensive, in-depth window tour of the 16 Mb line on floor 1. Everyone had to completely undress, take a water shower, gown, enter a transition area, then regown in a bunny-suit to enter the class 1000 space in the window area around the perimeter of the fab. The fab itself is ballroom style, with about 20 Nikon steppers evident in the center aisle. Mitsubishi said that they had about 50 CVD reactors in this fab. The total capacity is about 25,000 wafer starts per month. The most notable thing is the nearly complete dependence on automation. Also, none of the operators were wearing gloves. The other Mitsubishi facility in Kochi is also automated, but uses a different scheme, one more suitable for ASIC production. Mitsubishi did not provide further details.

At Saijo, wafers are stored in open carriers. Robots are flexible enough to move from 1 to 4 carriers. Stockers with elevators to move and store wafer carriers during processing were located in every bay. Each wafer carrier has a smart-card ID that accompanies it. The 24 wafers within a carrier may be broken into as many as 12 lots for individual control of processing. Robots, AGVs and a monorail system are exclusively used to move wafers (see Fig. 1). The robots material handling system was described as robust and is organized into main and branch systems. Elevators are used to transport wafer carriers between the floor and the monorail. The single overhead monorail rings the entire floor. In nearly 2 years of operation, Mitsubishi claims that the monorail has only been down twice, both times for minor repairs that were effected within a few hours. The monorail system was open, leading us to question particle contamination, but Mitsubishi denied this presented a problem. The move to complete factory automation was made to increase component yield. They seem convinced that the approach has been successful and is cost-effective but did not present the accompanying product yield data.

The organization and operation of the automated facility was openly discussed. The architecture is shown in Fig. 2. Nearly all of Mitsubishi's product and process design and development occur at the Kita-Itami works. Note the PBX connection between host computers. All of Mitsubishi's factories worldwide have similar communication systems. All planning and scheduling for the Saijo factory are performed at the local host level. The computer schedules maintenance and dispatches operators as necessary through alpha



MITSUBISHI ELECTRIC

FIG 1: The wafer carrier transportation system. The stocker has an elevator to move wafers between the overhead monorail and the equipment within the bay.

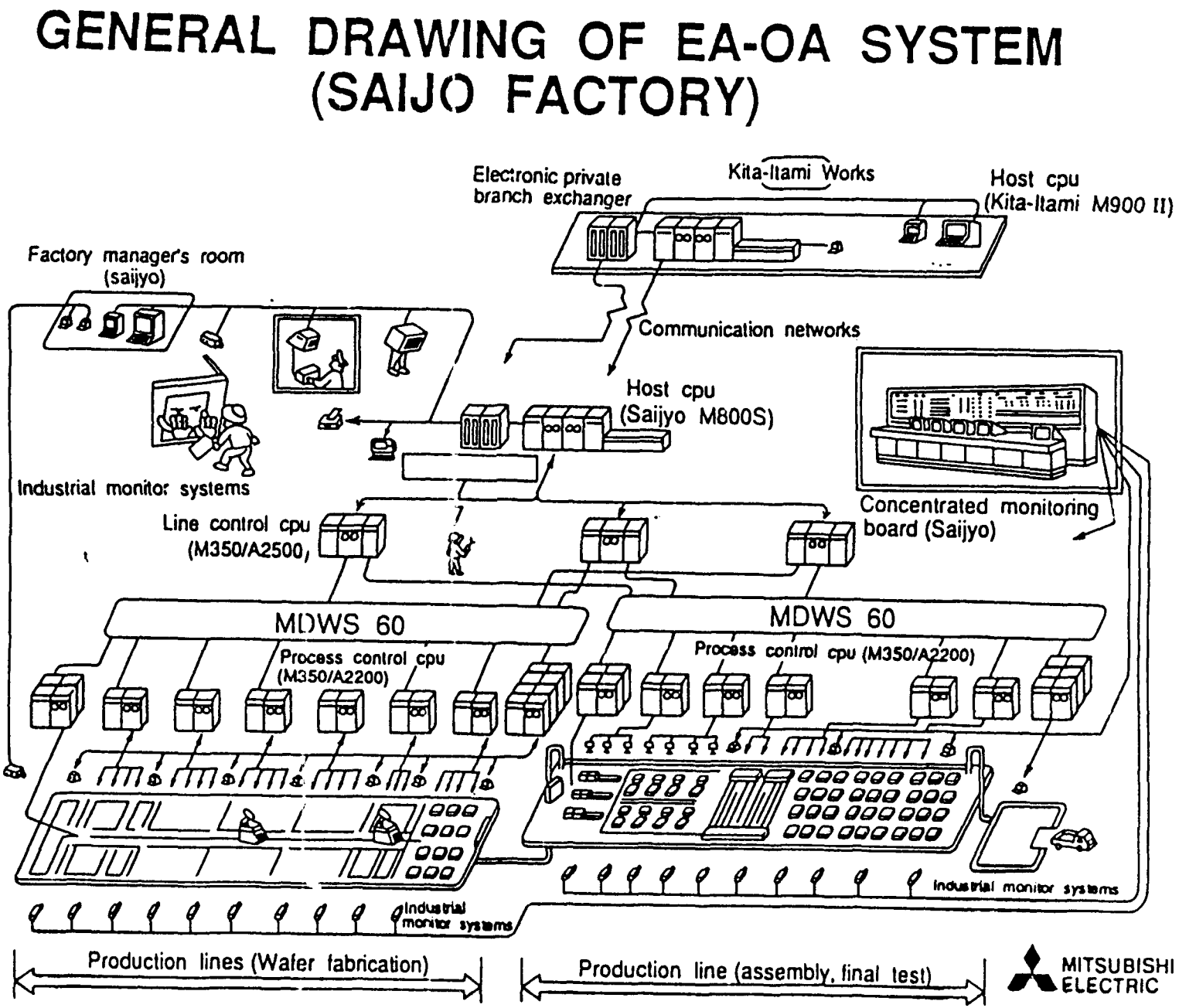


FIG 2: The architecture of the factory automation/control system at Saijo.

pagers. The Saijo line has a combined architecture where the product flows through a flow-shop while the machines are organized in a job shop.

Since yield enhancement was a driver for Mitsubishi to move to complete automation, the factory has an aggressive quality control system. The system tracks trends, provides control, and self-diagnosis. The architecture is shown in Fig. 3. Test results and data from each chip/wafer/lot tested are stored for 6 months on-line in an 8-10 Gb database on an HP9000 fileserver.

1.3 Ultra-Clean Technology

Mitsubishi appears to have an appreciation and acceptance of the importance of ultra-clean technology. A wide range of topics were described in this area, including both "defensive" and "offensive" approaches to improve conventional equipment and materials and develop new processes. The Mitsubishi strategy for addressing ultra-clean technology is shown in Fig. 4. Future trends and requirements were also described (see Fig. 5). One of the main challenges will be to improve the sensitivity of diagnostic tools for the detection of particles and contaminants. The vision of the ultra-clean facility of the future is shown in Fig. 6.

In building A, a class 1 facility, air is forced vertically at a flow of 0.38 m/s. Vibrations in the plant are below 0.5 μm. Deionized water has a resistivity of 18 MΩ-cm with less than 1 particle/cm^3. Particles within gases are below 1/ft^3. The dew point of gases are below -100° C. The oxygen impurity level of nitrogen is below 5 ppb. Hydrogen is generated on-site, while nitrogen is supplied by an outside company.

1.4 Additional Discussions

A member of Mitsubishi's technical staff from the planning department (Tokyo) presented an approach to solve the manufacturing planning/scheduling problem through simulation of factory performance. The software is used for prediction of work load and may, in the future, be used as an aid during factory design. It may also be used to suggest weekly release plans for wafers, a run takes about 15 minutes to execute. The approach is based on Petri net modeling techniques and displays results through Gantt charts. It was unclear how well developed and tested this particular code was, who uses it, and to what degree. Therefore, the utility and usefulness of the code was difficult to assess. In general, Mitsubishi said that they were implementing a modeling program to help solve problems relating to factory flexibility, i.e. what the best course of actions are if tools are down or if the number and type of products needed changes. The eventual goal of the modeling efforts are to develop codes that will assist Mitsubishi in factory design.

Mitsubishi discussed their target of spending $700 million for a future 20,000 wafer per month state-of-the-art facility. They see this as realizable for a

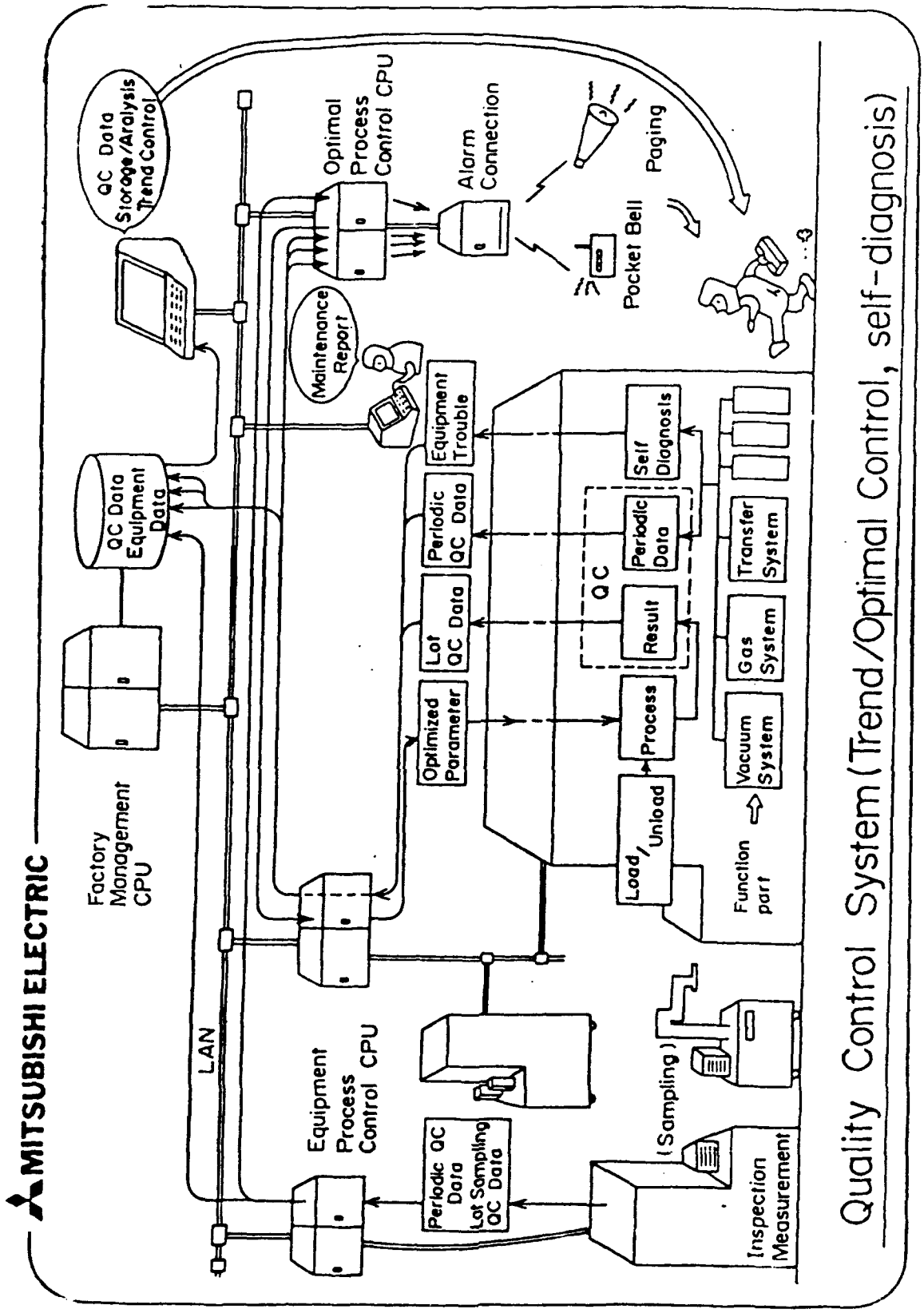


FIG 3: Architecture of the Mitsubishi quality control system at Saijo.

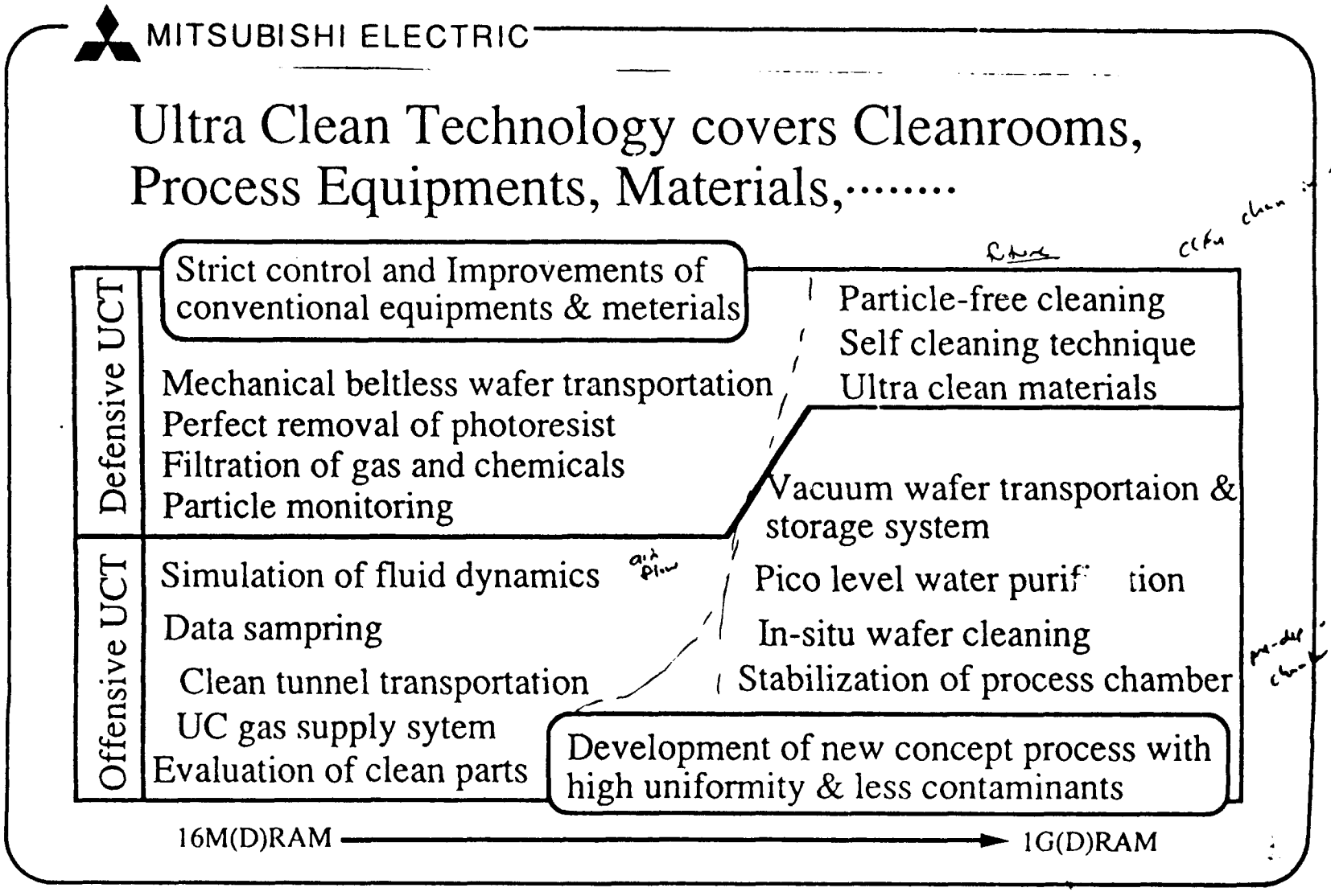


FIG 4: Mitsubishi strategy for ultra-clean technology.

MITSUBISHI ELECTRIC

FUTURE TREND

process design goals

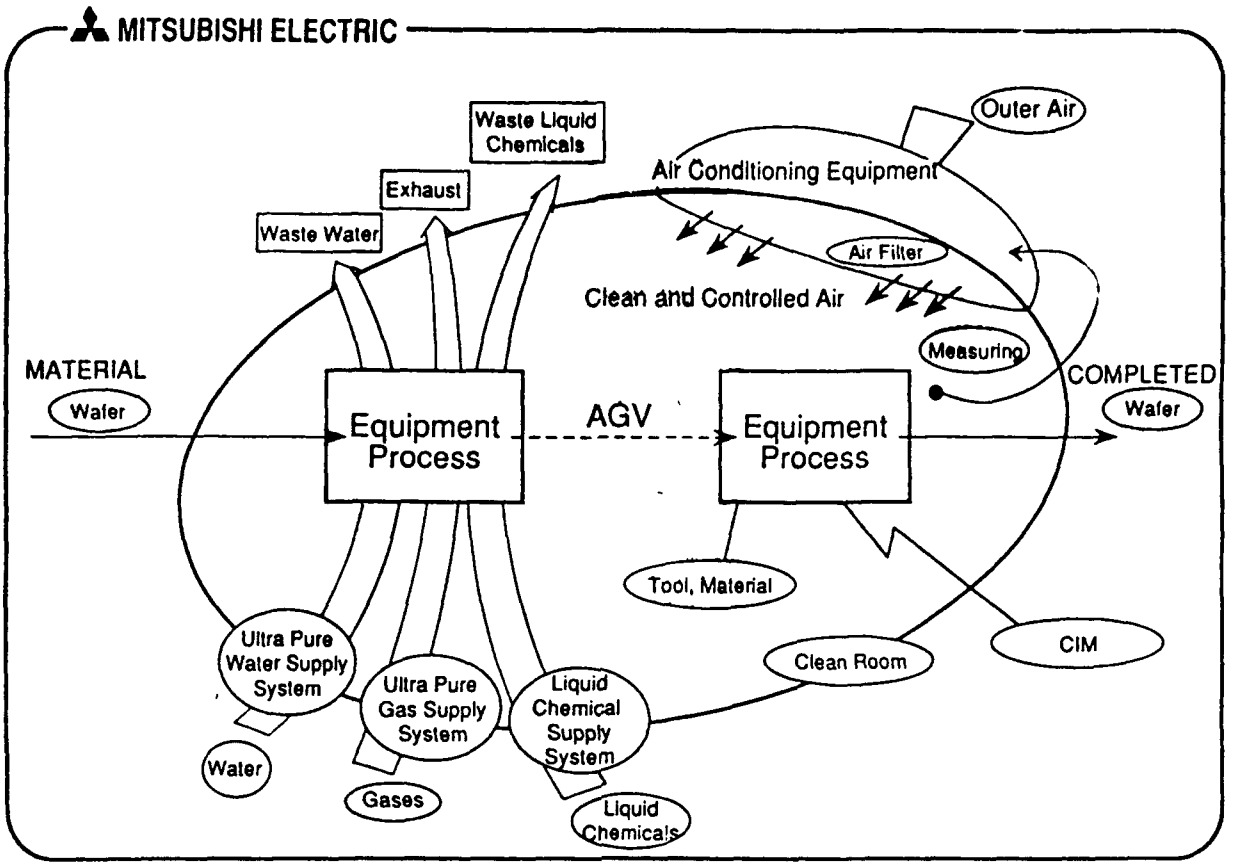
	16M(D)RAM 0.5 μm	64M(D)RAM 0.35 μm	256M(D)RAM 0.25 μm	1G(D)RAM 0.15 μm
Particle Size	.1~.05 μm	.08~.03 μm	.06~.02 μm	.04~.01 μm
Particle Density	0.02pc/cm^2	0.01pc/cm^2	0.005pc/cm^2	0.002pc/cm^2
Metal Contamination	10E10 atom/cm^2	7E9 atom/cm^2	5E9 atom/cm^2	3E9 atom/cm^2

DI H_2O TOC < 100 ppb

Silica < 1 ppb

Process gas < 1 particle/ft^3

FIG 5: Future trends of device geometries and particle limits.



MITSUBISHI ELECTRIC

Clean Technology ——— Future Theme

Main Item	Target
Clean Room	Fume,Mist,Gas Impurity control
Utility,Material	Metal Contamination decrease Particle Contamination decrease
Process,Equipment	Particle Contamination decrease
Evaluation,Analysis	Detection Limit improvement Yield-up quick feed-back
Cost	Reasonable

30% cost reduction target for next-gen fab

FIG 6: The Mitsubishi vision of the ultra-clean factory.

200 mm wafer diameter. They are interested in developing a common mask technology between DRAM and ASIC products and noted that some phase-shift strategies are not useful for both cases. They indicated some interest in excimer lasers for lithography. According to their belief, the expense of anti-reflective coatings may be mitigated through increases in equipment uptime.

2.0 Toshiba Corporation
Toshiba Oita Works
Oita, Kyushu Island

Toshiba had 1991 revenues of about ¥710 billion. Their capital investments in 1991 were about ¥100 billion, while in 1992 they were about ¥80 billion. Toshiba is the world's largest producer of DRAMs. Oita is located on Kyushu Island, south and east of Honshu. Many Japanese semiconductor firms are located there, giving it the nickname of "Silicon Island". The Toshiba Oita Works was established in 1970. Production reached 5 billion pieces in 1988 and 10 billion pieces in 1992. More than 3,000 part numbers are now manufactured there. Products include MOS DRAM and other logic components. Presently, the factory is shipping about 6 million pieces per month of 1 Mb DRAM, 5.5 million pieces per month of 4 Mb DRAM and about 70 million pieces per month of CMOS logic ICs. Total production is in the range of 110 million pieces per month. There are 5 clean rooms in the facility, the newest is used for 16 Mb DRAM production. Only wafer fabrication services are provided at this site. The team was permitted a window tour of the oldest DRAM line.

Worldwide, Toshiba has 9 other factories and one engineering center. Each factory is responsible for a complete product line. The facility Iwate plant has responsibility for ASIC production, while the Mie plant has responsibility for module production. There are 2 sites in southeast Asia for DRAM production near consumer electronics assembly areas.

2.1 Manufacturing Site Description

Toshiba's Oita works consist of 5 clean rooms and about 330,000 square meters of floor space. The oldest clean rooms, previously used for memories, are now used for CMOS logic components in the 3 μm range. Production of 1 and 4 Mb DRAM is done at 0.65 μm, as are some SRAM products. The newer lines use 6 inch wafer diameters, while others use 5 and 4 inch. The clean rooms in the 4 and 16 Mb lines are class 100. I-line exposure and phase-shift masks are used in the 16 Mb line. The 16 Mb line may be upgraded to accommodate 8 inch wafer diameters, since it is not yet fully equipped. About 1,600 people are employed in the clean rooms at this site, in 4 shifts.

Toshiba does not support and has not adopted Mitsubishi-style automation. Internally developed CIM systems are used, and internal software tools are used

to track hot lots and determine priorities. About 50 software support people are on-site and are totally occupied with maintaining and enhancing the present system. To integrate additional factory automation, more personnel would be required.

One interesting aspect of this site was the fountain located in the front. The water was treated waste water from the lines. It was pumped through the fountain to demonstrate its cleanliness, then discharged into a nearby stream. However, all other chemical waste was disposed of locally.

2.2 Facility Description

Toshiba took us on a window tour of the site's least advanced DRAM line, producing 1 Mb products and equivalent. Toshiba claimed that the 4Mb and 16 Mb facilities were very similar in most respects. The size of this facility was 129 by 66 meters and was divided into two mirror images. The building was three floors, test and measurements on floor 1, fabrication on floor 3, and air return and utilities on floor 2. About 50 different product numbers are produced there. The facility was organized in a conventional sense, into bays containing various manufacturing cells. G-line lithography was in use in this line. Many tools from U.S. suppliers were in use including Applied Materials, Varian, and Lam. Nikon steppers were seen as well. All tools were computerized to allow automatic download of recipes. Although the actual computer technology was not very advanced, it was extensive and well implemented on the factory floor. Toshiba informed us that most of the equipment used in the Oita fabs were computerized.

Wafers were stored in sealed containers. A single monorail system, in class 1000 space was used to transport wafers. No intrabay automation was used. Computer terminals, located within the bay, inform operators of lot locations and priorities. All equipment was computer controlled with automatic recipe download. Wafer lots were bar code and had paper travellers. Air monitors are located in each room and near each piece of equipment. A central monorail in class 1000 space was used to move wafers between bays. Elevators move wafers between floors.

Operators in the fab do not wear gloves, not even in the lithography area under most circumstances, according to our host. However, during our visit, an operator was observed donning gloves to handle a reticle. No air showers are used to enter the fab because Toshiba believes these may cause static charge buildup on operators. Instead, ion showers are used to remove particles from operators and garments. Equipment is maintained by Total Product Maintenance (TPM) teams.

3.0 Sony Corporation
Atsugi Technology Center
Atsugi, Japan

The Sony Semiconductor Group is broken into 4 business divisions, bipolar IC, CCD, MOS and Memory, and Compound Semiconductor. Within each division are quality assurance, production technology, design technology, materials distribution, and planning and control. Worldwide, there are 6 factories and one technology development center (Atsugi). Sales in the semiconductor group were about ¥190 billion in 1992, evenly mixed between merchant and captive supply. The product mix is 20% CCD, 30% bipolar, 30% logic, and 10% other. Sony expects a 15% increase in 1993 to about 210 billion. Sony Semiconductor is a relatively small supplier, presently number 18 in the world.

All process research and development occurs at Atsugi. Sony is not a major DRAM producer; their main memory components are SRAMs. Also, Sony accounts for about 60% the world's market of laser diodes, an area closely tied to sales of compact disc players and CD ROM machines. With the release of the new mini-disc format, this area may begin to expand. A brand new R&D center in the Atsugi center has just been completed for an 8 inch wafer line. The total cost of the building alone, no equipment, was about ¥20 billion. The center features 2 clean rooms, one class 1 and one class 10. Both have 2,376 square meters of floor space. The team was not permitted to view this facility.

3.1 Site Activity Description

The Sony R&D efforts are now focused on 0.35 μm device technology for products such as the 16 Mb SRAM, 2/3 inch 2 million pixel CCD imagers, 64 Mb non-volatile memory, and ASICs. Sony is developing i-line and excimer (KrF) lasers for exposure sources in lithography. Research is also being conducted on 0.25 μm devices and below. Products here include 64 Mb SRAM, 256 Mb DRAM, and 1/2 inch 2 million pixel CCD imagers. Excimer laser exposure sources are under research, as are low temperature etch, and high-purity processes. Other activities at the Technology Center include Technology-CAD, large diameter wafer processing, and advanced cleaning. Sony has not yet committed to any phase shift technologies. The site runs on one 8 hour shift.

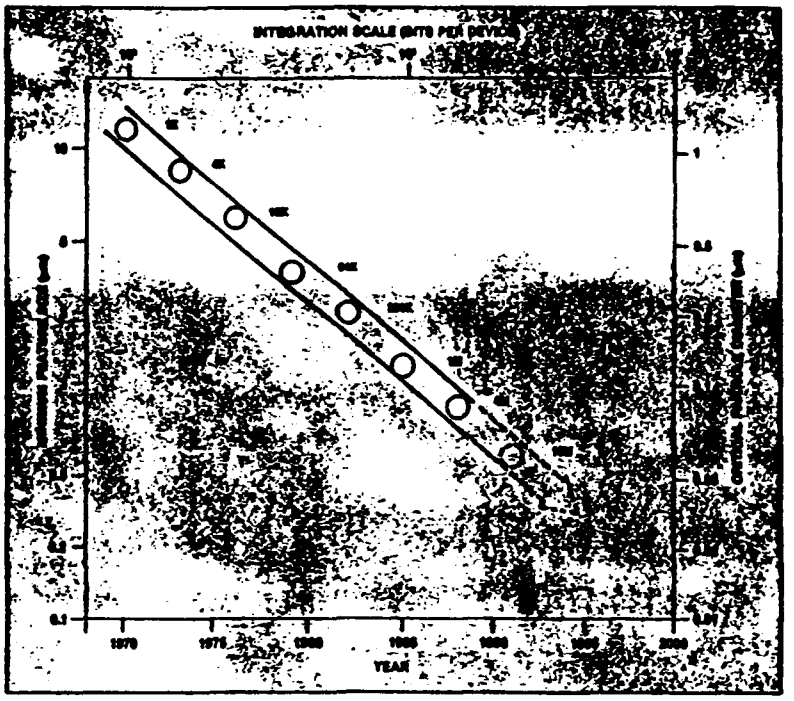
3.2 Facility Description

The team entered one of the research clean rooms. It contained mainly old equipment, an obvious research lab for silicon processing. The team also toured part of a separate clean room used for growing epitaxial doped GaAs layers on 2-3 inch GaAs wafers. Custom designed MOCVD reactors were seen. The reactors

(a)

(worst)	High-Current Ion Implanter
	Reactive-Ion Etcher
	Plasma Etcher
	Plasma-enhanced CVD
	⋮
	Wet Station
	Oxidation Furnace
	Coater/Developer
(best)	Stepper

(b)



(c)

TABLE 1 – POINT-OF-USE DEIONIZED WATER REQUIREMENTS FOR DRAM PRODUCTION

Requirement	ASTM (proposed 1983)	64K DRAM	256K DRAM	1M DRAM	4M DRAM
Resistivity (MΩ-cm)	>18	>17	>18	>18	>18
Particle count (number/mL)	<2 (1.0μm)	<50 (0.2μm)	<50 (0.1μm)	<30 (0.1μm)	<30 <10 (0.05μm)(0.1μm)
Living organisms (number/mL)	<1	<0.5	<0.2	<0.05	<0.01
TOC (μg/L)	<50	<500	<200	<50	<20
Oxygen (mg/L)	—	<0.2	<0.1	<0.1	<0.1
SiO_2 (μg/L)	<5	<20	<10	<5	<5

FIG 7: (a) Rankings of tools for particle generation; (b) Feature size and critical particle diameter vs. integration level; (c) requirements on deionized water.

were designed empirically and from Sony's past experience. The 13 employees that work here, 5 engineers and 8 technicians, are responsible for the development and production of over 60% of the world's supply of laser diodes.

3.3 Ultra-Clean Technology Discussion

Sony's approach to ultra-clean processing is to emphasize particle reduction at the wafer surface. They consider this very important for yield considerations. Results from an experimental study of particulate generation during processing is showed in Figure 7a. From the process-side, Sony is also researching methods to reduce process-induced contamination. An engineer (Dr. T. Hattori) from the Technology Center gave a brief presentation on ultra-clean technology. He gave his personal views on certain subjects, but could not commit Sony's intentions to follow. He admitted that his 10 year vision was very risky for the company to follow. He believes that there are compelling reasons to move to mini-environments, such as reduced maintenance, increased reliability, particulate free, standardization, and automation. There are also advantages to the use of tunnels between tools, although this approach leads to a nearly rigid, fixed process. Adoption of SMIF standards could add some flexibility. Also, use of redundant contamination free systems may be important for future clean rooms. Sony presented us with reprints of several papers on ultra-clean technology. The trend of feature size and critical particle diameter is shown in Fig. 7b. The requirements on deionized water are shown in Fig. 7c.

4.0 Tohoku University
Sendai, Japan

The team visited two semiconductor research facilities, both under the direction of Professor Tadahiro Ohmi. One facility, called the "Super Clean Room", was claimed to be class 0.0001, or less under static conditions. Research in this facility is mainly on silicon for 0.1 μm processing. Research is supported by the Ministry of Education and several companies. In the second facility, called the "Super Mini-Clean Room", research activities are more closely related to studies of clean rooms themselves, as well as advanced tools, and processes. The team held lengthy discussions with Professor Ohmi and Associate Professor Shibata regarding ultra-clean manufacturing. Ohmi has developed an extensive strategy for next-century manufacturing. The overall concept is shown in Fig 8.

4.1 Super Clean Room

The Super Clean Room was located at the laboratory for Microelectronics, Research Institute of Electrical Communication, in an area of Sendai apart from the campus of the University. The clean room is housed in a relatively new, three story building. The clean room is on the second floor, to allow a nearly completely vertical air flow through the work area. The entire clean room and its contents,

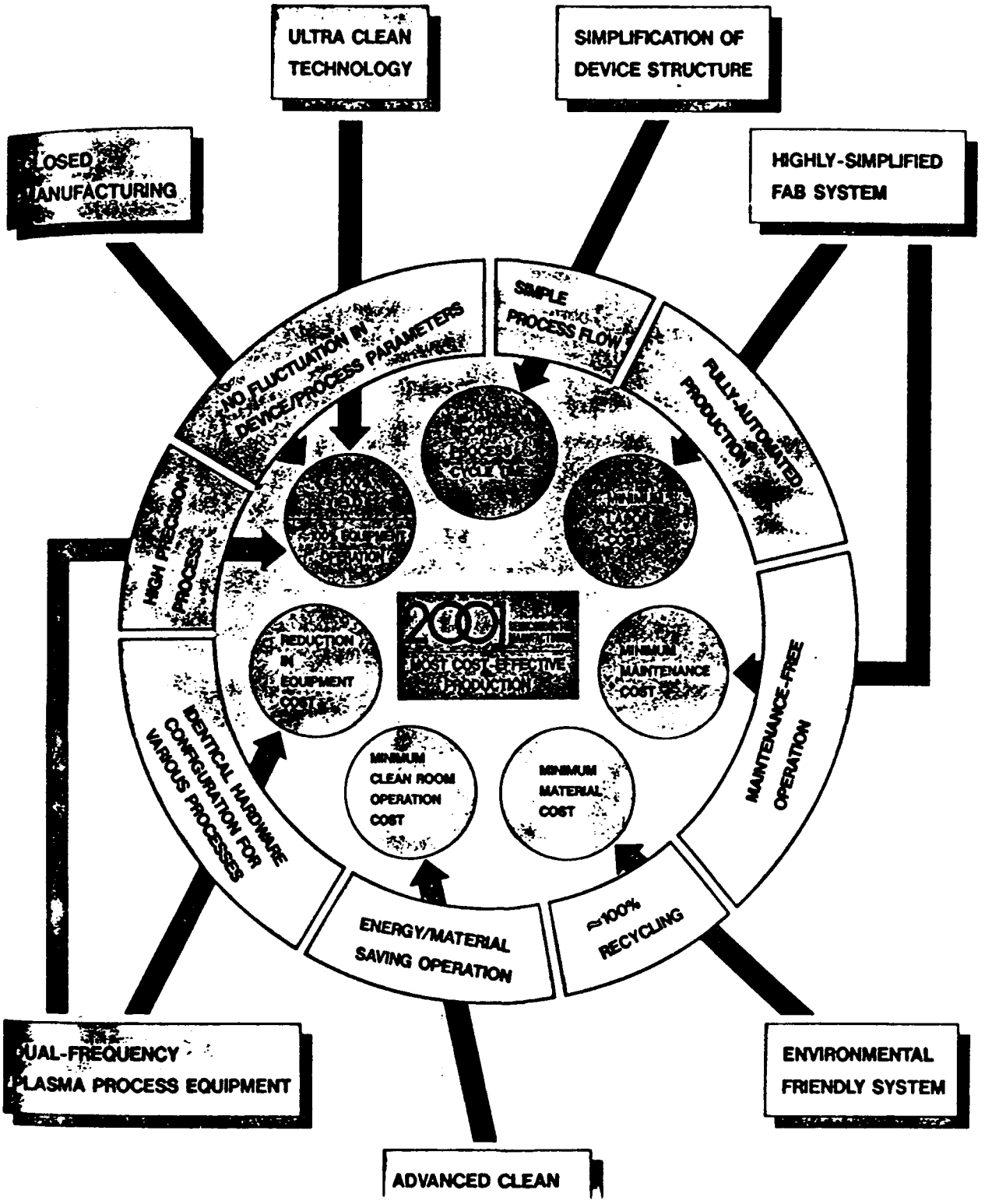


FIG 8: Overview of the Tohoku University proposal for manufacturing in 2001.

including operators, are grounded. The grounding scheme ensures that the maximum potential difference due to static charge buildup is limited to under 5V. The projects under research in this facility are aimed at solving process issues for 0.1 μm geometries. There are 5 basic areas under investigation: Silicon IC, optical IC, high frequency analog IC, hybrid IC (SAW devices), and Josephson IC.

Funding for the Super Clean Room comes from 2 sources. The Ministry of Education provided the start-up costs of ¥200 million (¥20 million for building, ¥80 million for clean room, and ¥100 million for equipment) and provides about ¥20 million in annual support. This money is now mainly used to support maintenance and operations of the facility. Additional support is provided by companies through their research laboratories. Presently eleven companies are participating on projects there. Within the facility, 11 Professors and 40 students and about 200 other people use the clean room. The team toured the inside of this clean room. It was obviously a prototyping laboratory for device and process development work.

4.2 Discussion with T. Ohmi

The team met with Professor Ohmi and Associate Professor Shibata, both from the Electrical Engineering Department. Ohmi's research program has adopted a 10 year vision. He has on-going projects in many areas, from advanced device design and development to process R&D to advanced equipment and ultra-clean technology.

Ohmi's strategy for future semiconductor issues is fairly well known since he publishes regularly in English-language journals and attends conferences and meetings. We openly discussed his program for solving the problems of the next decade. He believes that there are 6 key issues (summarized in Fig. 9) to achieve the most cost-effective production in the future. These issues are:

1. simplified device structures,
2. equipment productivity enhancement,
3. ultra-clean wafer surface preparation,
4. perfect process - parameter control in processing,
5. standardized equipment,
6. common reticle production for various ASICs.

Solutions to these key issues will allow manufacture of high-yield lots from the beginning, without depending on volume-learning to perfect the process. He sees ultra-clean technology and process control as key here. He is suggesting the use of closed tunnels, either in vacuum or nitrogen, between equipment to isolate wafers from environmental air. The concept is shown in Fig 10 in the case of cluster tools (also a concept Ohmi supports). Standards are seen as very important for the industry to reduce the cost of future equipment. Since about 65% of the cost of a factory is the capital investment in the equipment (10% is in

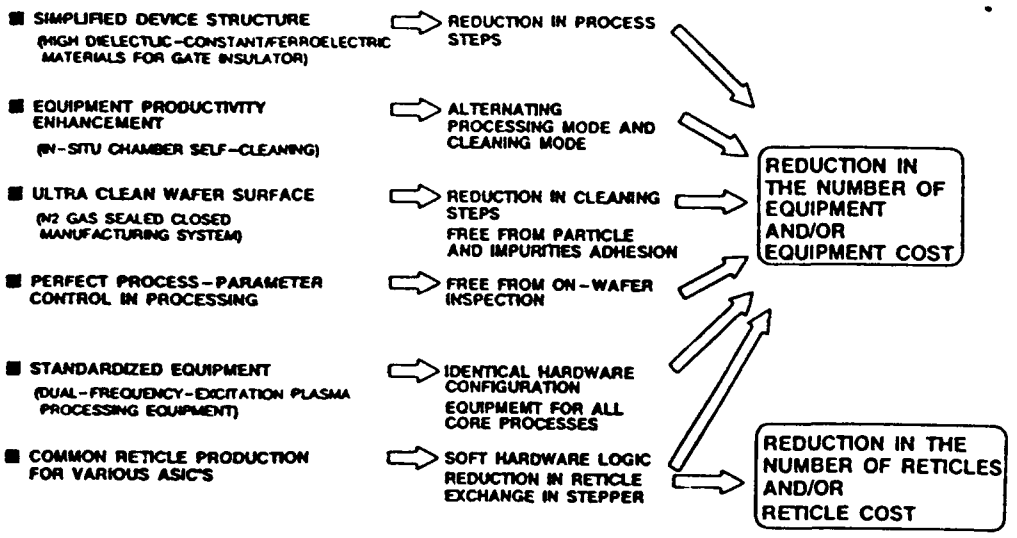


FIG 9: Summary of the key issues to realize cost-effective production of semiconductors.

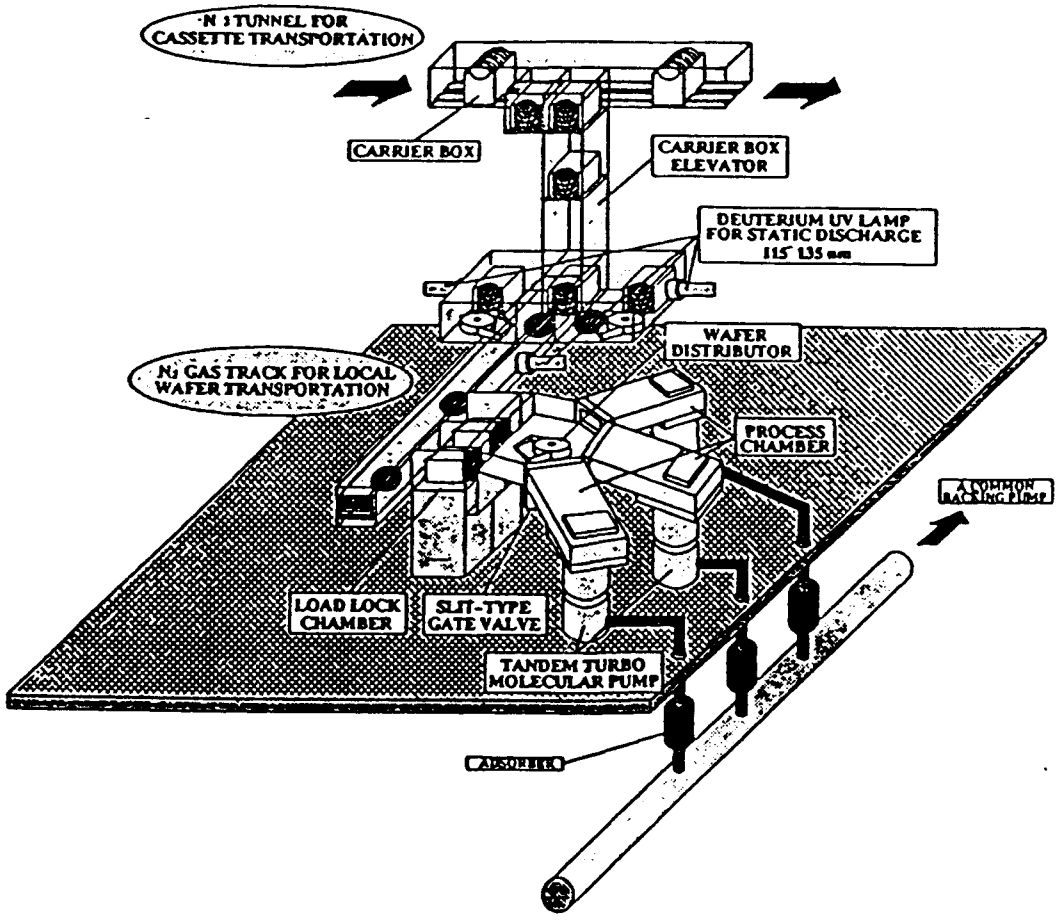


FIG 10: Example of a nitrogen tunnel, shown here with cluster tools.

installation, the rest is in the facility construction and utilities), reductions here, through standardization and mass-production of common components can obviously have a significant effect on reducing the total cost.

His group is investigating a new 4-terminal device structure to address issue number 1. This new structure called the "neuron MOSFET" utilizes a floating gate and potentially may allow a great reduction in the number of gates necessary to implement a Boolean logic function. However, this type of device may not lead to substantially reduced processing, but it may reduce the total number of interconnects. ASIC circuit architectures based on this transistor can also allow a reduction in the number of reticles required since the circuit function is determined by electrical signals, rather than processing. Ohmi's group is also investigating other device structures and materials to simplify processing, including insulators with high-dielectric constants and ferroelectrics.

Another area of investigation is particle adhesion within reaction chambers. Ohmi is researching low pressure processing to avoid generating particles in the gas phase within the process chambers. He is also examining self-cleaning techniques to remove particulates prior to loading wafers. Yet another approach under investigation is weakly charging thin films to prevent adhesion. The most obvious solution to the adhesion problem is to eliminate particulates.

Work at the University has led to the development of a passivation technology that provides a corrosion-resistant surface. The university holds patents on processes to use Cr_2O_3 and CrF_3 treatments of gas lines and chambers. The benefits of Cr_2O_3 and CrF_3 passivation have been verified experimentally. Creation of a high-quality passivation layer, about 150 Å thick, requires careful surface preparation. Along the same lines, the group has investigated welds and fittings for gas lines. They have developed welding procedures that require much shorter bead lengths, thereby decreasing surface areas for impurities. Inspection-free gas fittings that contain instruments to detect leaks have been patented and have the potential to reduce installation and monitoring costs. Due to U.S. environmental laws and codes, some of this technology could not be applied domestically.

To address issues relating to the high cost of equipment due to low utilization, his group is developing a tool that can be used for multiple major process steps. A cross-section of the tool, called the Dual-Frequency Excitation Plasma Process Equipment, is shown in Fig. 11. Two rf sources are used to control ion flow from the inlet, one source biases the wafer while one excites the plasma. Adjusting the frequencies and powers of the sources, as well as the inlet gas, allows the tool to operate in different regimes, including sputtering, RIE, plasma CVD, resist ashing, and dry cleaning. This tool also may provide precise control over critical process parameters during manufacturing.

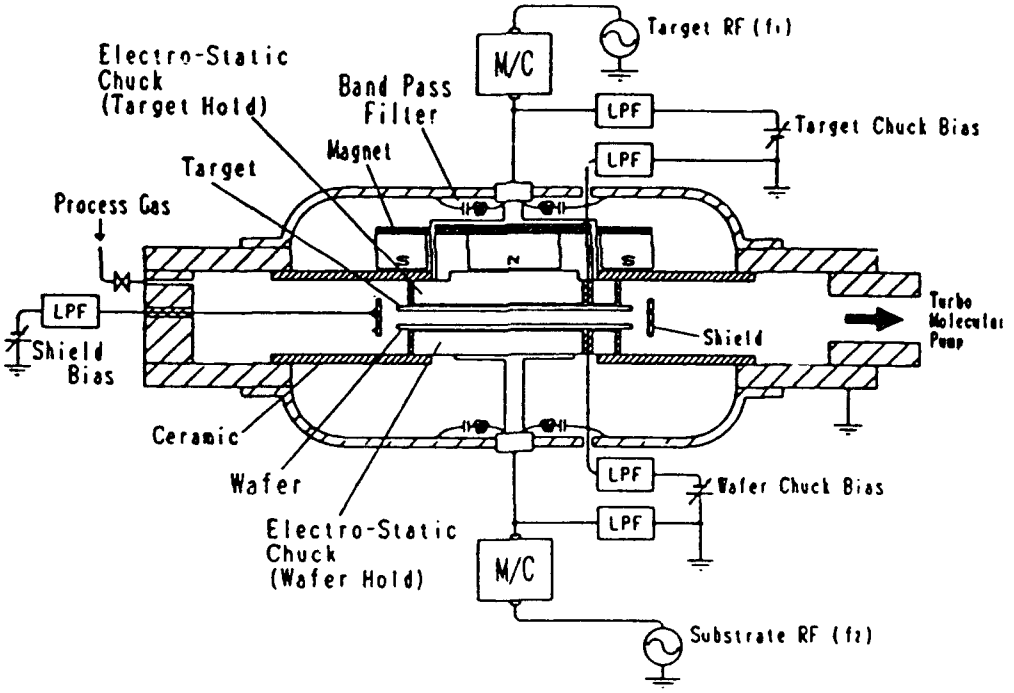


FIG 11: The Dual Frequency Excitation Plasma Reactor.

4.3 Super Mini Clean Room

The Super Mini Clean Room is located on the campus of Tohoku University. The Super Mini Clean Room is used by staff, students, and outside researchers. Ohmi tries to build a collaborative team among his group, bringing personnel from competitors together to exchange ideas and work together. He believes that the approach has been successful. The clean room is set up as a basic research laboratory and has many areas set aside for process experiments. Many of Ohmi's concepts are investigated and proven-out here with the staff of students and outside researchers from equipment suppliers and semiconductor companies. A US chemist from Air Products (a US company) was participating on one of Ohmi's projects and discussed his research with us.

The facility itself is inside of a previously existing 1 story building. Truly vertical air flow could not be achieved, but is approximated by returns along the perimeter. Returns are created by acrylic sheets impregnated with carbon fibers for grounding. The sheets allow flexibility of the room configuration within the research area. many of Ohmi's ideas are tested and implemented here. The Dual Frequency Excitation Plasma Process Equipment was shown to us, as well as an advanced wet cleaning station to prevent contamination and native-oxide growth during cleans. Other experiments shown to us included improvements in the pumping scheme for a low pressure chamber and the water purification and deionizing schemes.

5.0 Fujitsu Limited
Kawasaki, Japan

The team met with technical and managerial staff from Fujitsu Limited at an R&D facility in Kawasaki. The meeting did not include a tour of any clean rooms. The discussions were quite interesting and covered a range of topics. Fujitsu is not only a producer of semiconductors, but is also a large producer of computers and related equipment (displays, disc drives, etc.). Fujitsu's net sales were about ¥2.5 trillion last year and they employed about 50,000 people. Electronics devices were responsible for about ¥350 billion of the total business and employ about 13,000 of the employees in 18 plants. Fujitsu explained company organization and described research goals. Fujitsu also communicated their concern over rising semiconductor manufacturing costs. Company goals are to develop the capabilities to have less than 1 week turnaround for an ASIC and 2 days for a gate array. Fujitsu works with suppliers to develop tools, but will not cooperate with other semiconductor companies on standard requirements. They issue specifications and expect their suppliers to meet them. There is presently a 6 year development time for tools, but Fujitsu believes it could be halved. Fujitsu will license patents to suppliers, but they may not use them on tools sold to competitors. Fujitsu made it quite clear that they speak only to suppliers, never to competitors.

5.1 Fujitsu Overview

Fujitsu Limited consists of 5 groups and Corporate Administration. The Electronic Devices Group is responsible for all of Fujitsu's production of semiconductor components. Within this group, the Product Group is broken into Compound Semiconductors, Memory LSI Design, Process, Engineering Development, LSI Quality and Reliability, Hybrid IC, Electromechanical Devices, and Display. There are 14 plants in Japan, and 6 in the rest of the world.

The newest clean room is located in Mie. Fujitsu initially agreed to grant the team access to this facility, but later decided against it. However, SEMATECH has visited this plant and reported it to be a single-wafer ASIC mega-fab. The Fujitsu Manager responsible for designing the ASIC line in the Mie plant told us that the line had been designed for purely fastest turn-around. It was originally just a pilot production plant, but was now being converted to handle a greater production capacity. The plant at Wakamatsu is the newest and has the most advanced ASIC line, although the plant is not highly automated. The lithography area in the Iwate plant is Fujitsu's most advanced. Presently using G-line for 0.6 μm features. I-line will be used for 0.5 -0.4 μm features, and possibly smaller with phase shift masks. DUV is under consideration for the following generations.

The technology transfer within Fujitsu Limited is accomplished by transferring personnel. For example, key engineers might move first from Kawasaki to Mie, then from Mie to Iwate, Wakamatsu, or Aizu. The final destination depends on the type of product.

Fujitsu Laboratories Limited is a wholly owned subsidiary. It has capital of about ¥5,000 million and 1,650 employees. It operates 3 facilities, Kawasaki, Atsugi, and an International Institute. Electronics research occurs in Atsugi in the Electron Device Division, the Electronics System Division, the Materials Division, and the Optical Interconnect Division. In the Electron Device Division, activities include:

Design:	processors, CAD systems
Devices:	sub 0.2 μm CMOS, SOI, HEMT
Processes:	lithography, contamination control, high dielectric constant materials

In the Electronics System Division, activities include electron beam testing. In the Materials Division, activities include ceramics, MCM, photoresists, and characterization techniques.

Additional research on superconductors and applications is under investigation. For example, Josephson devices for LSI, millimeter wave, and x-

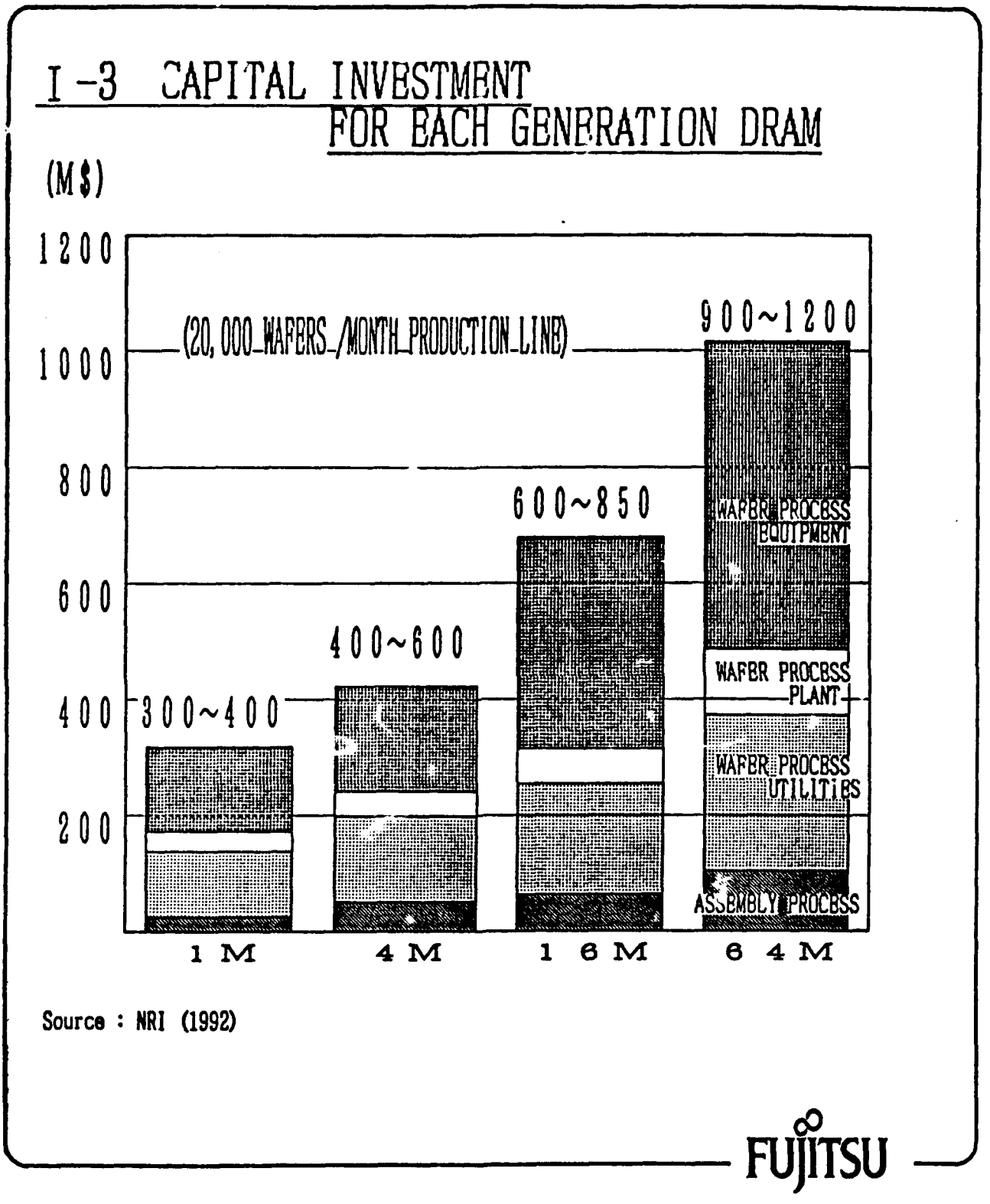


FIG 12: Capital investment for DRAM factories (Fujitsu).

ray detection applications. CMOS research goals are,

-"scaling MOS" by 1994
-"epi-channel MOS" by 1997
-"double-gate SOI MOS" by 2000.

5.2 Equipment Discussions

The team held a discussion over Fujitsu's view of the future in the industry. Figure 12 shows Fujitsu's estimates of capital expenditures for factories. Fujitsu estimates the capital investment for a 20,000 wafer per month, 64 Mb DRAM plant to be $900 - 1,200 million. About 50% of the cost is due to the equipment. A plant of this nature for mass production may utilize large wafer diameters of 12 inches or more, and should be flexible enough to be capable of processing diversified devices. On the other hand, Fujitsu noted that about 50% of the ASIC lots contained fewer than 5 wafers. Fujitsu showed us data indicating that throughput efficiency decreased non-linearly with wafer lots under 5 wafers (see Fig. 13). ASIC production includes about 3000 different part numbers, 300 different designs, and 30-40 different processes.

On the equipment side, a further examination of the cost breakdown showed that about 60 - 70% of the cost of a piece of equipment is due to the processing part, the rest is due to the CIM and transportation system. Standardization in these components would reduce equipment costs substantially, according to Fujitsu. There are no SEMATECH-like program to bring Japanese semiconductor firms together to develop a set of standard requirements on tools, but there is some activity to discuss standards through SEMI and EIAJ. Fujitsu has an in-company standardization of equipment. Further moduling of equipment might have additional benefits. Areas that are well suited for standardization of modules are valves and piping, vacuum gauges and mass-flow controllers. The wafer carrier interface could be standardized, both the physical station and the procedures. Finally, Fujitsu sees some benefit in standardizing operation manuals.

To improve the performance of equipment in a mass production floor, equipment suppliers must improve the uniformity and repeatability, and reduce the particles. Device designers must better match designs with equipment capabilities. For small lots typical of ASIC production, equipment suppliers must introduce tools that feature pre-cleaning, in-situ control, target changes under vacuum, no wafer breakage, robust recipe download capabilities. Device and process designers must design products based on a standard process and begin combining small lots to increase throughput efficiencies. Issues common to both mass production and ASIC are perfect- processing and efficiency improvement. Fujitsu sees three factors leading to the greatest increases in efficiency,

- improvement of product yield,
- improvement of uptime and throughput, and
- reduction of operators.

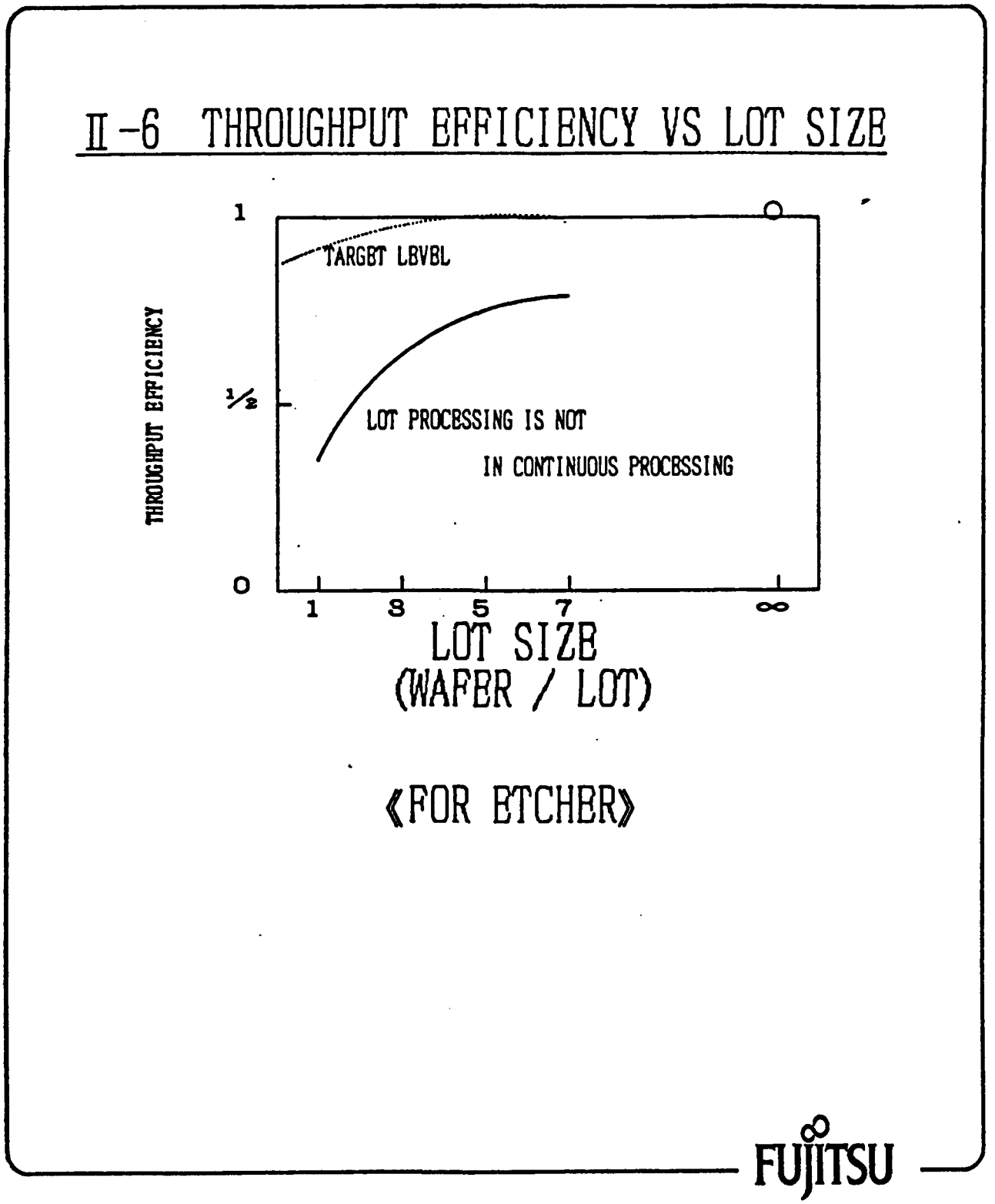


FIG 13: Graph of tool efficiency vs. lot size (ASIC case).

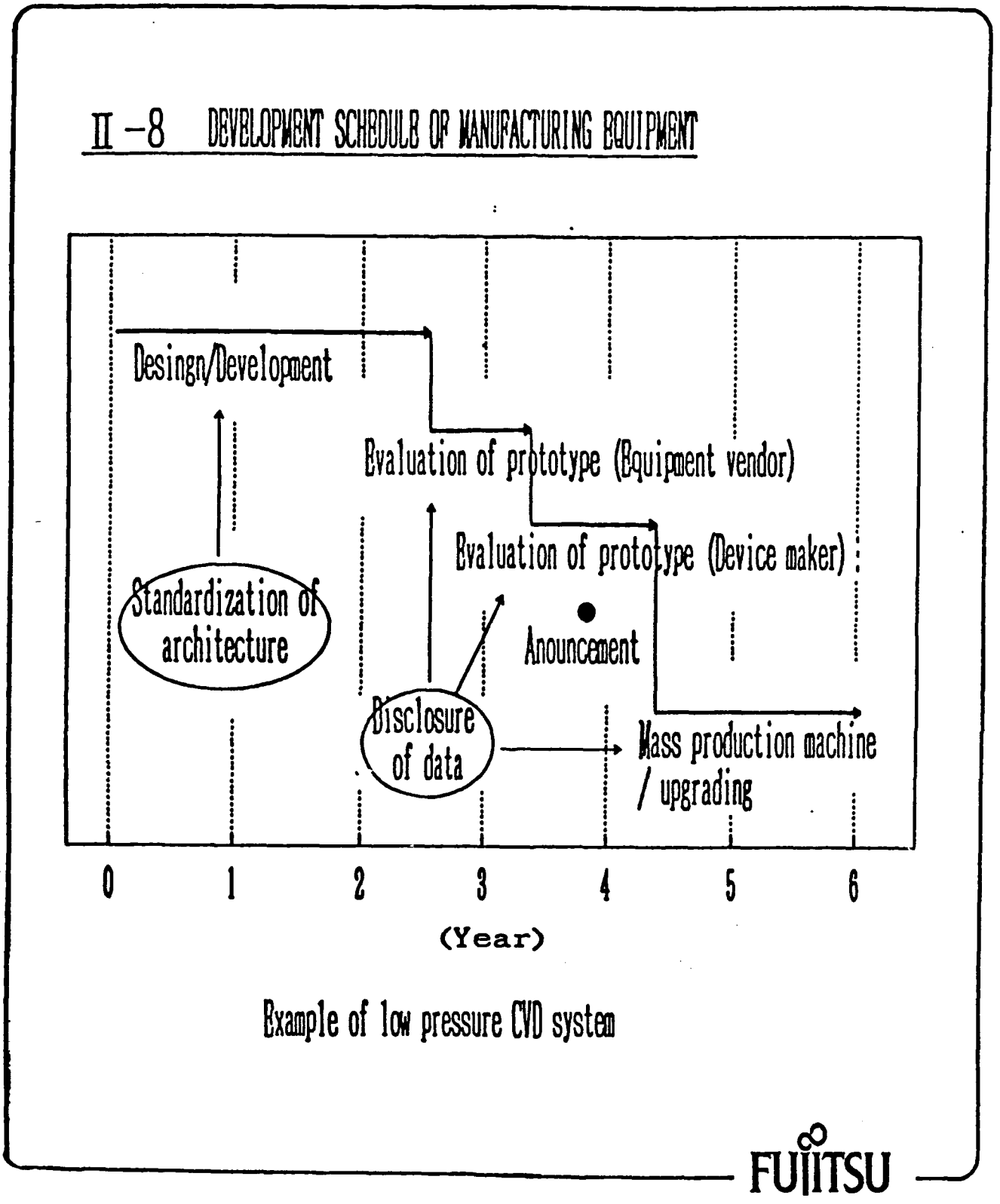


FIG 14: Typical tool development schedule.

As shown in Fig. 14, during the present 6 years it takes to develop new equipment, Fujitsu sees the need for greater disclosure and sharing of data between semiconductor companies and suppliers. By better utilizing this data, it is hoped that both uptime and time to market of new tools will be increased. Equipment suppliers could facilitate this by utilizing an open design architecture and open control software, and by sharing maintenance and service data. Manufacturers should disclose tool performance data and uptime information. Fujitsu also sees the need for much more effective training of operators.

Fujitsu does not believe that the approach put forth by Professor Ohmi will prove to be cost-effective. They do believe that ultra-clean technology is important, but they feel one must address yield directly, not just reduce particle levels. They acknowledge that Tohoku University could be quite valuable as a neutral site to bring companies together to discuss standards.

List of Japanese Participants

MICHIYO SHINDO
MANAGER, GENERAL & COMMERCIAL
PLANNING & ADMINISTRATION DEPARTMENT
ELECTRONIC DEVICES GROUP

MITSUBISHI ELECTRIC CORPORATION
2-2-3, MARUNOUCHI CHIYODA-KU, TOKYO 100, JAPAN
PHONE(03)3218-3607 FAX(03)3218-2936

Dr. TAKAYUKI MATSUKAWA
MANAGER
WAFER FABRICATION DEPT. B

MITSUBISHI ELECTRIC CORPORATION
SAIJO FACTORY
8-6, HIUCHI, SAIJO CITY, EHIME PREFECTURE, 793 JAPAN
PHONE: (0897)55-1821 FAX:(0897)53-2950

SHIGEO UOYA
DEPUTY MANAGER
IC PROCESS ENGINEERING DEPT.

MITSUBISHI ELECTRIC CORPORATION
KITA-ITAMI WORKS
4-1 MIZUHARA ITAMI CITY HYOGO, 664 JAPAN
PHONE: 81 727 { 84 7101 (DIRECT) FAX: 81 727 72 6592
82 5131 (COMP.)

Dr. MAKOTO TSUKIYAMA
SENIOR RESEARCHER
ADVANCED SYSTEMS GROUP

INDUSTRIAL ELECTRONICS & SYSTEMS LABORATORY
MITSUBISHI ELECTRIC CORPORATION
1-1, TSUKAGUCHI-HONMACHI 8-CHOME, AMAGASAKI, HYOGO, 661 JAPAN
PHONE: (+81 6) 497-7640 FAX (+81 6) 497-7727
E-mail:tsukiyama@soc.sdl.melco.co.jp

MITSURU YAMADA
MANAGER
WAFER FAB. ENGINEERING SECT. B
WAFER FABRICATION DEPT. B

MITSUBISHI ELECTRIC CORPORATION
SAIJO FACTORY
8-6, HIUCHI, SAIJO CITY, EHIME PREFECTURE, 793 JAPAN
PHONE: (0897)55-1811 FAX:(0897)53-2950

HIROTOSHI ANDO
PLANNING & ADMINISTRATION DEPARTMENT
ELECTRONIC DEVICES GROUP

MITSUBISHI ELECTRIC CORPORATION
2-2-3, MARUNOUCHI CHIYODA-KU TOKYO 100, JAPAN
PHONE(03)3218-3318 FAX(03)3218-2936

HARUOMI OKUNO
PLANNING & ADMINISTRATION DEPARTMENT
ELECTRONIC DEVICES GROUP

MITSUBISHI ELECTRIC CORPORATION
2-3, MARUNOUCHI 2-CHOME CHIYODA-KU, TOKYO 100, JAPAN
PHONE: 03-3218-3647
FAX 03-3218-2936(G3) 03-3223-8439(G4)

TOSHIBA

YOSHIHISA MAKITA

SENIOR MANAGER
PRODUCTION AND MATERIALS CONTROL

TOSHIBA CORPORATION OITA WORKS
3500 MATSUOKA, OITA CITY, OITA PREF. 870-01, JAPAN
PHONE:(0975)24-8040
FACSIMILE:(0975)20-4028

SONY

Dr. Takeshi Hattori
General Manager
Ultraclean Technology Process Technology
ULSI R&D Laboratories

Sony Corporation Atsugi Technology Center
4-14-1, Asahi-cho, Atsugi-shi,
Kanagawa-ken, 243 Japan
Telephone 0462-30-5461 Fax 0462-30-5572
Telex 3872306SONYAT J

SONY

Dr. Shoji Hirata
Manager
R&D Coordination Dept
R&D Corporate Planning Group

Sony Corporation
6-7-35, Kitashinagawa
Shinagawa-ku, Tokyo, 141 Japan
Telephone 03-3448-3176 Fax 03-3448-7811-5708

SONY

Dr. Morikazu Konishi
Senior Engineer
ULSI R&D Group

Sony Corporation Atsugi Technology Center
4-14-1, Asahi-cho, Atsugi-shi,
Kanagawa-ken 243 Japan
Telephone 0462-30-5912 Fax 0462-30-6419

SONY

Masahide Mitsuoka
~~Assistant~~ Manager
R&D Strategy Dept
R&D Corporate Planning Group

Sony Corporation
6-7-35, Kitashinagawa
Shinagawa-ku, Tokyo, 141 Japan
Telephone 03-3448-2657 Fax 03-3448-7811-5708

Hajime Yagi
Senior General Manager
ULSI R&D Laboratories

Sony Corporation
Atsugi Technology Center
4-14-1 Asahi-cho
Atsugi-shi Kanagawa-ken 243 Japan
Phone (0462) 30-5372
Fax (0462) 30-6374

SONY

Akiko Kikuchi
R&D Administration Department
Corporate Planning Group

Sony Corporation
6-7-35, Kitashinagawa
Shinagawa-ku, Tokyo, 141 Japan
Telephone 03-3448-3557 Fax 03-3448-7811-5708

PROF. TADAHIRO OHMI
DIV.
OF SOLID STATE ELECTRONICS

DEPARTMENT OF ELECTRONICS
FACULTY OF ENGINEERING
TOHOKU UNIVERSITY,SENDAI 〒980
TEL 022(224)2649(OFFICE)
022(225)6656(HOME)
FAX 022(224)2549

DR. TADASHI SHIBATA
ASSOCIATE PROFESSOR
SOLID STATE ELECTRONICS LABORATORY

DEPARTMENT OF
ELECTRONIC ENGINEERING
TOHOKU UNIVERSITY
AZA-AOBA, ARAMAKI, AOBA-KU, SENDAI 980, JAPAN
PHONE:(022)224-2649(WORK), 245-4786(HOME)
FAX (022)224-2549

MIZUHO MORITA, Ph. D.
ASSOCIATE PROFESSOR
FIRMWARE SCIENCE LABORATORY

DEPARTMENT OF
INFORMATION SCIENCE
TOHOKU UNIVERSITY
SENDAI 980, JAPAN

SUPER CLEAN ROOM
PHONE : 022-227-9088
FAX : 022-227-8089

Raymond N. Vrtis, Ph.D.
Senior Research Scientist
Electronics

AIR PRODUCTS

Air Products and Chemicals, Inc.
Visiting Researcher at Tohoku University
Professor Ohmi's Laboratory
Aza-Aoba, Aramaki, Aobaku, Sendai 980, Japan
Phone/Fax: 022-263-9395 (Work)
Phone/Fax: 022-211-1381 (Home)

MASANAO ITOGA

GENERAL MANAGER
MANUFACTURING TECHNOLOGY DIV.
ELECTRONIC DEVICES GROUP

FUJITSU LIMITED

1015, KAMIKODANAKA NAKAHARA-KU,
KAWASAKI 211, JAPAN (Company Mail No./E130)
TEL. (044) 754-2480 FAX. (044) 754-2848

Dr. Yasutaka Ban

Deputy General Manager
Electron Device Group and
Corporate Technology Advancement Group

FUJITSU LIMITED

1015, KAMIKODANAKA NAKAHARA-KU,
KAWASAKI 211, JAPAN (Company Mail No./E2301)
TEL. (044)754-2480 FAX: (044)754-2585
NIFTY-Serve RHE00083

TAKAHIKO MISUGI, Ph. D.

PRESIDENT AND REPRESENTATIVE DIRECTOR

FUJITSU TECHNO RESEARCH LIMITED

KOSUGI FUJITSU BLDG.
1812-10, SHIMONUMABE, NAKAHARA-KU,
KAWASAKI, 211, JAPAN
TEL. KAWASAKI (044) 433-8113 FAX. (044) 433-8117

AKIRA ABIRU

DEPUTY GENERAL MANAGER
MANUFACTURING TECHNOLOGY DIV.
ELECTRONIC DEVICES GROUP

FUJITSU LIMITED

1015, KAMIKODANAKA NAKAHARA-KU,
KAWASAKI 211, JAPAN (Company Mail No./E130)
TEL. (044) 754-2473 FAX. (044) 754-2848

MINORU INOUE

ASSISTANT TO MANAGER
1ST MANUFACTURING TECHNOLOGY DEPT.
MANUFACTURING TECHNOLOGY DIV.
ELECTRONIC DEVICE

FUJITSU LIMITED

1015, KAMIKODANAKA NAKAHARA-KU, KAWASAKI
211, JAPAN (Company Mail No./E252)
TEL (044) 754-2514
FAX (044) 754-2792

Dr. TAKASHI ITO

MANAGER
SEMICONDUCTOR DEVICES LABORATORY

FUJITSU LABORATORIES LTD.

10-1, MORINOSATO-WAKAMIYA,
ATSUGI 243-01, JAPAN
TEL (0462) 48-3111
FAX (0462) 48-3473

HAJIME ISHIKAWA

DIRECTOR
ELECTRON DEVICES DIVISION

FUJITSU LABORATORIES LTD.

10-1, MORINOSATO-WAKAMIYA,
ATSUGI 243-01, JAPAN
TEL: (0462) 50-8803
FAX: (0462) 48-3896

Distribution

ARPA

Dr. Gary Denman,	Director
Dr. Duane Adams,	Deputy Director
Mr. Sven Roosild,	Acting Dir., Microelectronics Technology Office
Library	

ONR

Dr. Albert Wood,	Code 4400
Dr. Fred Saalfeld	Code 1001
Dr. Bruce Robinson,	Code 3000
Dr. Arthur Bisson,	Code 4000
Dr. Paul Quinn,	Code 4410
Dr. Eli Zimet,	Code 4410
Dr. Sachio Yamamoto,	Director, ONR Asia Office
Dr. Victor Rehn,	Scientist, Semiconductor and Surface Physics, ONR Asia Office

DoD

Dr. Bill Bandy,	Director, Microelectronics Research Lab
Mr. Richard Bernstein,	Scientist, DIA
Mr. Jack Bachkosky,	USD(A), DDR&E, Dep. Director
Mr. Jim Compton,	USD(A), Dep. Under Sec'y (International Programs), Prin. Ass't Deputy (International Programs)
Mr. Carl Baker	USD(A), DDR&E, Special Ass't to Dep. Director
Mr. Bruce Bade,	USD(A), Dep. Under Sec'y (International Programs), Ass't Dep. Under Sec'y (International Development & Prod. Programs), Dir., Far East Programs
Dr. Rodney Tanaka	Dir., Defense Technology Office, Mutual Defense Assistance Office, US Embassy, Japan